DiskOnModule

Hi-Speed DJ Series

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pqi

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Copyright Information

Symbol Description

- ● : Special information
- ● : Need to keep caution
- Warning : Need to be careful

1. Product Description

1.1 Product Overview

PQI's DiskOnModule (DOM) is the storage device based on NAND flash memory technology. This product complies with 40 PIN IDE (ATA) standard interface and is suitable for data storage media and code storage device for embedded system and boot disk. By using **DiskOnModule,** it is possible to operate good performance for the systems, which have IDE interface.

With small form factor, the applicable appliance can add or install IDE storage device on its Mother Board or Complete set.

● **Application Fields;**
- ■ Industrial PC and Thin Client
- ■ Game and Telecommunication Machine
- ■ Ticketing, Examining, testing machine
- ■ Army, Health and Production Equipment and Machine

1.2 Product Features
- ● Small form factor with IDE (ATA) Standard Interface connector
- ● Memory Capacities: 32MB ~ 6GB
- ● High performance and reliability
- ● Noiseless and stable installation to system
- ● Operating voltage 3.3V or 5.0V operation
- ● Standard IDE (ATA) Interface
- ● Master and Slave Switch
- ● Write Protection Switch
- ● Operating as Boot Disk
- ● Data Storage Device to 6GB
- ● Code Storage Device for Embeded Operating System

1.3 System Requirement
- The Host system which is connected to DiskOnModule should meet system requirements at minimum;

1.3.1 Power Requirement
- ● Voltage: DC +3.3V ± 5% or DC +5.0V ± 10%

1.3.2 Operating System
- ● Windows 2000/XP
- ● Linux
- ● DOS
- ● WinXP Embedded
- ● WinCE

1.3.3 Interface
- ● IDE (ATA) Standard Interface

2. Specification

2.1 Physical Specifications

2.1.1 Overlook
The overlook views of DiskOnModule are illustrated in Figure 1.

Write Protect Switch   Power Connector   Master/Slave Switch
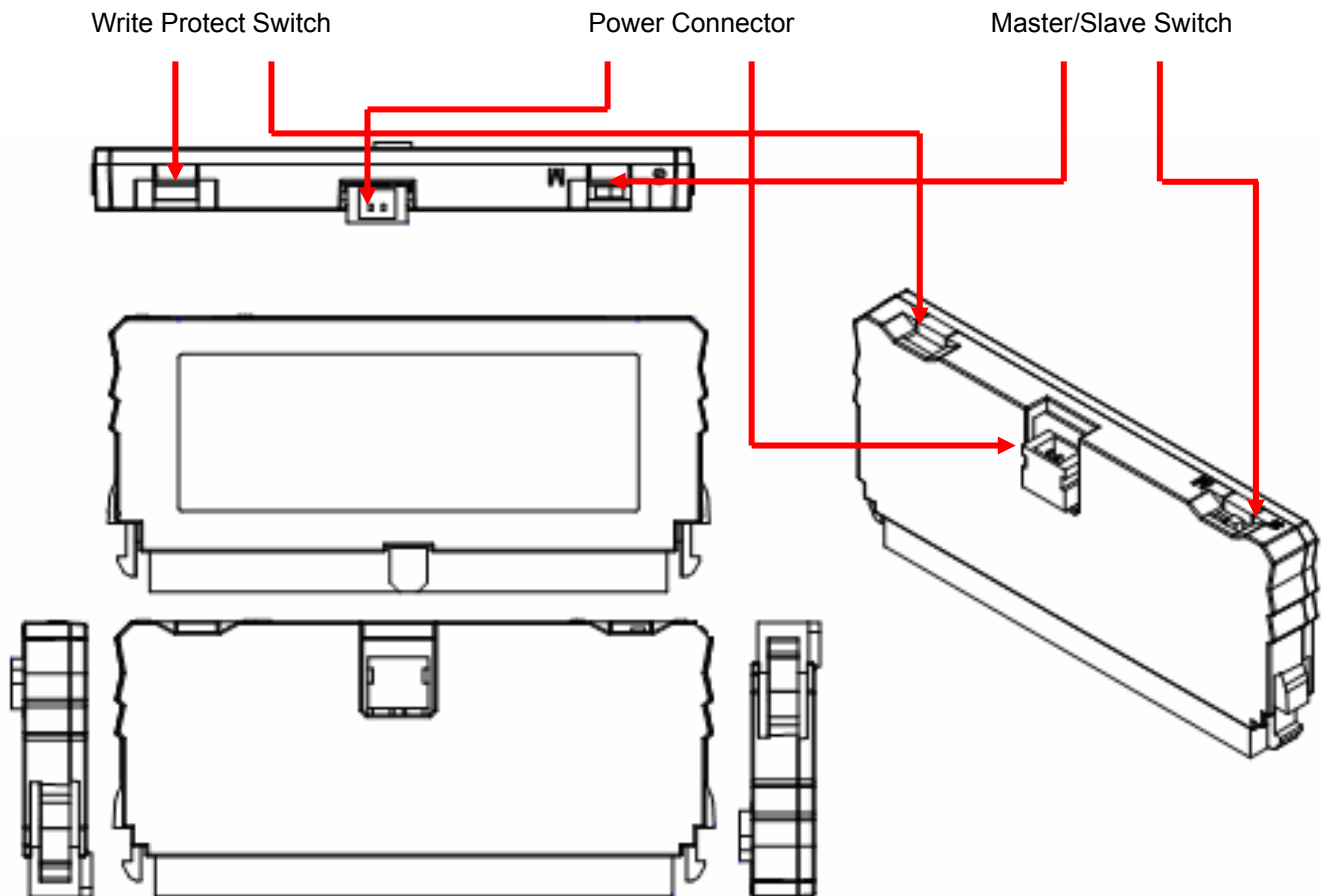
Figure 1: DiskOnModule Overlook Diagram

2.1.2 Dimension

The Dimensions of DiskOnModule are illustrated in Figure 2 by type.

DJ0XXXX22XX0 (40 PIN)
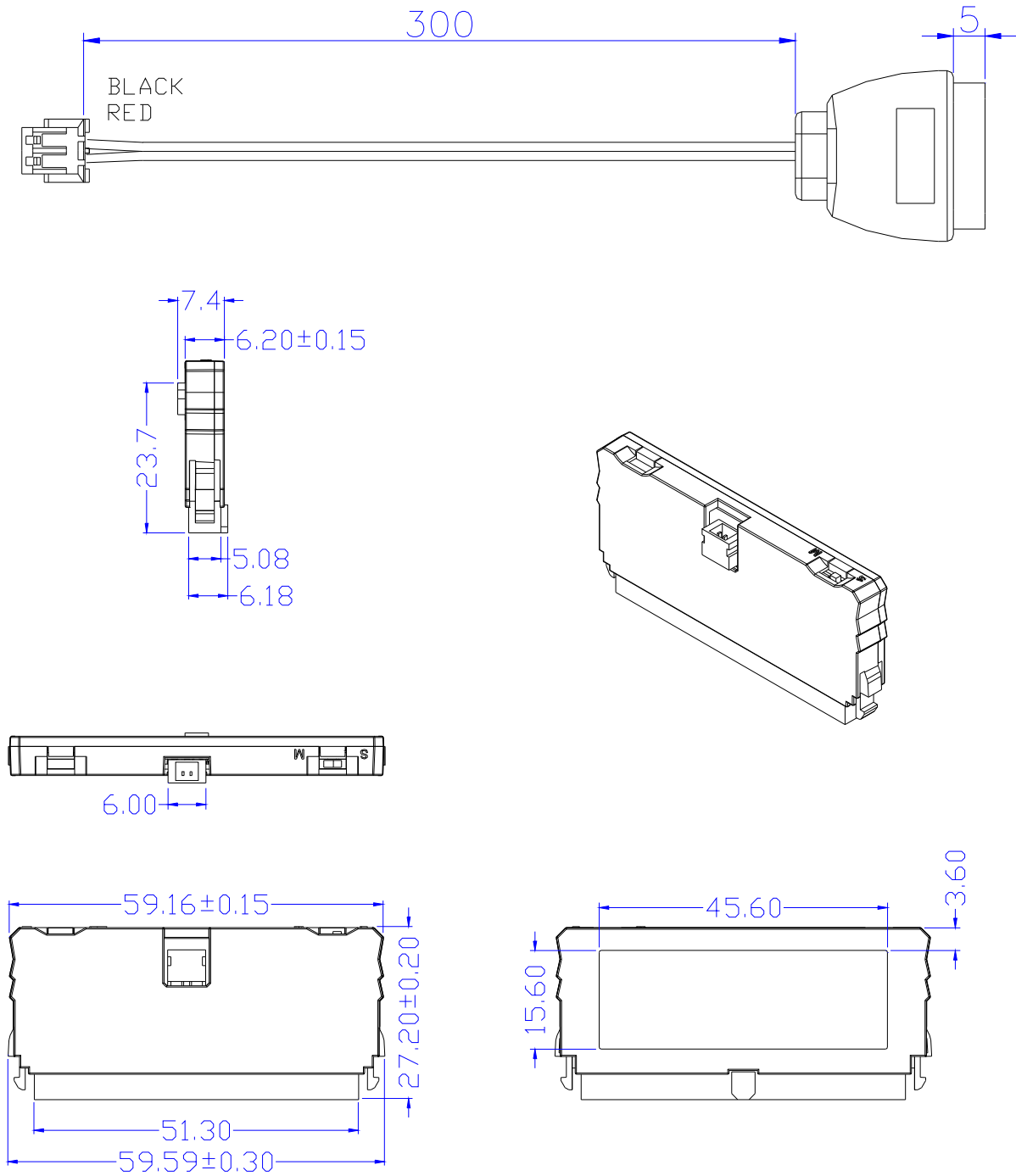
Figure 2: DOM Dimensions

Table 1: DiskOnModule Physical Dimension

Length	59.2 ± 0.2 mm
Width	27.2 ± 0.2 mm
Thickness	6.2 ± 0.2mm

2.1.3 Weight
- DiskOnModule Weight: < 12g
- Power Cable Weight: < 11g

2.2 Electronic Specifications

2.2.1 Product Definition
DiskOnModule is designed to operate and work as Data or Code Storage device by NAND Flash Memory and its Controller through IDE (ATA) Standard Interface to Host Systems.
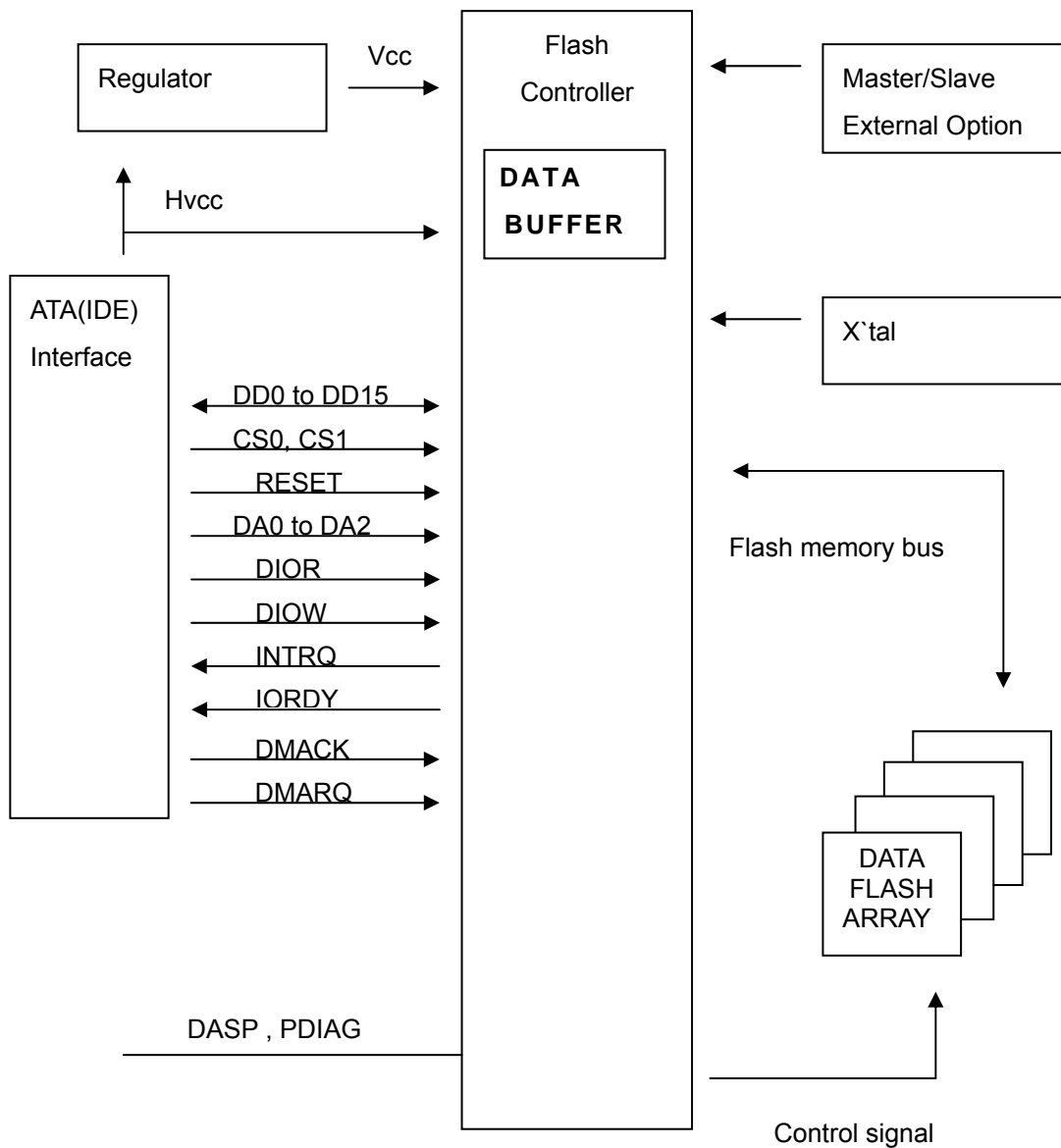
Figure 3: DiskOnModule Block Diagram

2.2.2 Operating Voltage
- Voltage DC +3.3V ± 5% (Option) or DC +5.0V ± 10%

2.2.3 Capacity and Block Size information
- Capacity: 32MB ~ 6GB
- Sector Size: 512B

2.2.4 Power Consumption
- DC Information
  Read: <15mA (Typ.), Write: <20mA (Typ.), Sleep: <3mA (typ.)
  [Notice] The value is various bases on the testing platform.

2.3 Performance Specifications

2.3.1 Modes
- Multi-Word DMA2
- PIO mode 4

2.3.2 Seek Time
- DiskOnModule has no seek time by being based on Flash Memory technology.

2.3.3 Mount Time
The Mount Time for initializing and mounting DiskOnModule is different by depending on Operating System and testing Platform.

2.3.4 Data Transfer Time
- Sequential Read: 7 MB/sec
- Sequential Write: 5 MB/sec

※ *Test Platform: GIGA 8I945GME Intel:945+ICH7 3.0GHz DDR:400*
Testing Software: HD Bench 3.4 Testing OS: Windows XP
[Notice] The value is various bases on the testing platform.

2.3.5 Data Retention
- 10years without requiring power support

2.3.6 Wear-leveling
- Dynamic Wear-Leveling for same level of Write/Erase Cycle

2.3.7 Bad Block Management
- The Bad Blocks of Flash Memory will be replaced into new ones by controller.

2.4 Environmental Specifications

2.4.1 Temperature
- Operating Temperature: 0ºC to +70ºC, Non Operating Temperature: -40ºC to +85ºC (Industrial type)

2.4.2 Humidity
- Operating Humidity: 10% to 95%
- Non-Operating Humidity: 10% to 95% (with no condensation relative humidity)

2.4.3 Vibration
- Random Vibration (Operation) : Testing Specification

Frequency (Hz)	PSD (G2/Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.01		30min per axis
100	0.08	6Grms	(X・Y・Z)
500	0.08		

- Sine Vibration (Non-Operation) : Testing Specification

Testing Specification		
Frequency（Hz）	Acceleration（G）	Dwell Time（min）
10~500 Hz	15 G	30min per axis (X・Y・Z)

2.4.4 Bare Drop Testing
- Testing Conditions: 75cm height
- Testing Orientation: (Free fell) Front/Rear/Right/Left/Top/Bottom side
- Testing Result: Pass

2.4.5 Shock and Altitude
    T. B. D.

2.5 Reliability Specifications

2.5.1 ECC/EDC (Error Correction Code/Error Detection Code)
- 2bytes data per 251bytes will be corrected.

2.5.2 Read and Write/Erase Cycle
- Read: No Limitation
- Write/Erase: 5,000,000 times
  (Estimated on reference to Doc No.SM070001)

2.5.3 MTBF (Mean Time Between Failure)
- 2,000,000 hours
  (Estimated on reference to Doc No.SM070002)

2.6 Compliance Specifications
- CE
- FCC

※ *Note: Please contact your closest PQI's office for other certificate information.*

3. Function

3.1 Switch Setting
 3.1.1 Master/Slave Switch
● On case which the switch place "Master" side, then the DOM will be recognized as C: Drive in system and operate as main storage device.
● On case of placing in "Slave" side, the DOM will be recognized as slave disk and operate as slave storage device.
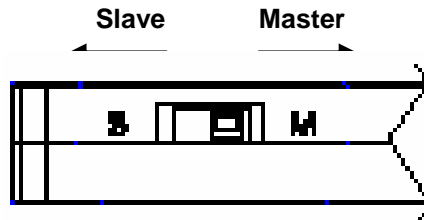
Figure 4: Master/Slave Function Switch

3.1.2 Write Protect Switch
● On case which the switch place "Lock" side, then the data can not be written into DOM and can be read only.
● On case of placing in "Unlock" side, the data can be written and read together.
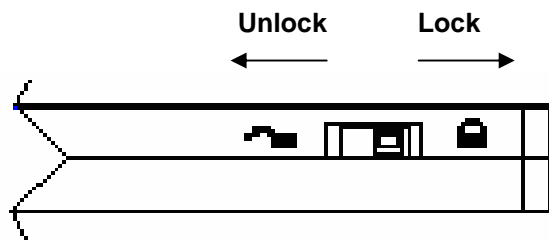
Figure 5: Write Protect Switch

3.2 Pin Signal Assignment
● The signals assigned for ATA applications are described in Table 2

Table 2: ATA connector pin definitions

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin) or Vcc
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground

※ Notes:

1. All pins are in a single row, with a 2.54 mm (0.100") pitch.

2. The comments on the mating sequence apply to the case of backplane blind mate connector only. In this case, the mating sequences are:

• - the pre-charge power pints and the other ground pins.

• - the signal pins and the rest of the power pins.

Pin 1   **Pin 39**

Pin 2   **Pin 40**
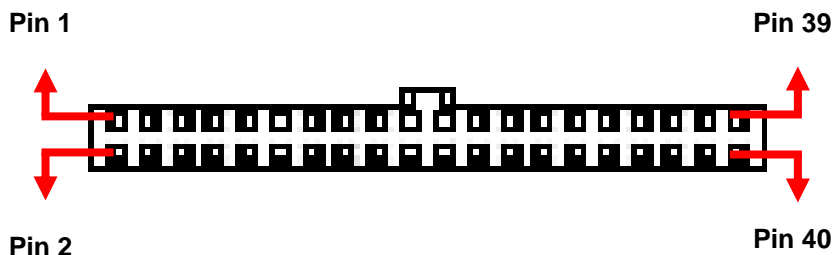
Figure 6: Signal Connector

3.3 Capacity Specifications

Table 3: Capacity Specifications

Capacity	Cylinder	Head	Sector	Total sectors
32MB	500	8	16	64000
64MB	500	8	32	128000
128MB	500	16	32	256000
256MB	1000	16	32	512000
512MB	1015	16	63	1023120
1024MB	2031	16	63	2047248
1536MB	3047	16	63	3071376
2048MB	4063	16	63	4095504
3072MB	6095	16	63	6143760
4096MB	8146	16	63	8211168
6144MB	12190	16	63	12287520

3.4 Interface Signal Assignments and Descriptions

Signal summary

The physical interface consists of receivers and drivers communicating through a set of conductors using an asynchronous interface protocol.

Table 4: Interface signal name assignments

Description	Host	Dir	Dev	Acronym
Cable select		(see note)		CSEL
Chip select0		→		CS0-
Chip select1		→		CS1-
Data bus bit 0		⇔		DD0
Data bus bit 1		⇔		DD1
Data bus bit 2		⇔		DD2
Data bus bit 3		⇔		DD3
Data bus bit 4		⇔		DD4
Data bus bit 5		⇔		DD5
Data bus bit 6		⇔		DD6
Data bus bit 7		⇔		DD7
Data bus bit 8		⇔		DD8

Data bus bit 9	⇔	DD9
Data bus bit 10	⇔	DD10
Data bus bit 11	⇔	DD11
Data bus bit 12	⇔	DD12
Data bus bit 13	⇔	DD13
Data bus bit 14	⇔	DD14
Data bus bit 15	⇔	DD15
Device active or slave (Device 1) present	(see note)	DASP-
Device address bit 0	→	DA0
Device address bit 1	→	DA1
Device address bit 2	→	DA2
DMA acknowledge	→	DMACK-
DMA request	←	DMARQ
Interrupt request	←	INTRQ
I/O read	→	DIOR-
I/O ready	←	IORDY
I/O write	→	DIOW-
Passed diagnostics	(see note)	PDIAG-
Reset	→	RESET-
NOTE – See signal descriptions for information on source of these signals		

3.5 Signal Descriptions

CS0 - (CHIP SELECT 0)
This is the chip select signal from the host used to select the Command Block registers.

CS1 – (CHIP SELECT 1)
This is the chip select signal from the host used to select the Control Block registers.

DA2, DA1, AND DA0 (DEVICE ADDRESS)
This is the 3-bit binary coded address asserted by the host to access a register or data port in the device.

DASP – (Device active, device 1 present)
This is a time-multiplexed signal which indicates that a device is active, or that Device 1 is present. This signal shall be an open collector output and each device shall have a 10 kΩ pull-up resistor.
If the host connects to the DASP- signal for the illumination of an LED or for any other purpose, the host shall ensure that the signal level seen on the ATA interface for DASP- shall maintain VOH and VOL compatibility, given the IOH and IOL requirements of the DASP- device drivers.

DD (15:0) (Device data)
This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers.

DIOR - (Device I/O read)
This is the read strobe signal from the host. The falling edge of DIOR- enables data from the device onto the signals, DD (7:0) or DD (15:0). The rising edge of DIOR- latches data at the host and the host shall not act on the data until it is latched.

DIOW- (Device I/O write)
This is the Write strobe signal from the host. This rising edge of DIOW- latches data from the signals, DD (7:0) or DD (15:0), into the device. The device shall not act on the data until it is latched.

DMACK- (DMA acknowledge)
This signal shall be used by the host in response to DMARQ to initiate DMA transfers.

DMARQ (DMA request)

This signal, used for DMA data transfer between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

This line shall be released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress. When enabled by DMA transfer, it shall be driven high and low by the device.

When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

INTRQ (Device interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the device has a pending interrupt, the device is selected, and the host has cleared the nIEN bit in the Device Control register. If the nIEN bit is equal to one, or the device is not selected, this output is in a high impedance state, regardless of the presence or absence of pending interrupt.

The pending interrupt condition shall be set by:
— the completion of a command; or
— at the beginning of each data block to be transferred for PIO transfers except for the first data block for FORMAT TRACK. WRITE SECTOR(S), WRITE BUFFER, and WRITE LONG commands.

The pending interrupt condition shall be cleared by:
— assertion of RESET-; or
— the setting of the SRST bit of the Device Control register; or
— the host writing the Command register; or
— The host reading the Status register.

IOCS 16- (Device 16-bit I/O)

Obsolete.

IORDY (I/O channel ready)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.If actively asserted, the signal only be enabled during DIOR-/DIOW- cycles to the selected device. If open collector, when IORDY is not negated, it shall be in the high-impedance (undriven) state.

This use of IORDY is required for PIO modes 3 and above and otherwise optional.

PDIAG - (Passed diagnostics)

This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. A 10 kΩ pull-up resistor shall be used on this signal by each device.

The host shall not connect to the PDIAG-signal.

RESET- (Device reset)

This signal from the host system shall be asserted beginning with the application of power and held asserted until at least 25 µs after voltage levels have stabilized within tolerance during power on and negated thereafter unless some event requires that the device(s) be reset following power on.

ATA devices shall not recognize a signal assertion shorter than 20 ns valid reset signal. Devices may respond to any signal assertion greater than 20 ns, and shall recognize a signal equal to or greater than 25µs.

CSEL (Cable select)

The device is configured as either Device 0 or Device 1 depending upon the value of CSEL.

3.6 Interface Register Definitions And Descriptions

Device addressing considerations

In traditional controller operation, only the selected device receives commands from the host following selection. In this standard, the register contents go to both devices (and their embedded controllers.) The host discriminates between the two by using the DEV bit in the Device/Head register.

Data is transferred in parallel either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisy chained on the interface, commands are written in parallel to both devices, and for all except the EXECUTE DEVICE DIAGNOSTICS command, only the selected device executes the command. On an EXECUTE DEVICE DIAGNOSTICS command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Devices are selected by the DEV bit in the Device/Head register. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected. When devices are daisy chained, one shall be set as Device 0 and the other as Device 1.

I/O register descriptions
Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA (2:0), DIOR-, AND DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device. The Control Block Registers are used for device control and to post alternate status.

Anytime a command is in progress, that is, from the time the Command register is written until the device has ompleted the command and posted ending status, the device shall have either BSY or DRQ set to one. If the Command Block registers are read by the host when BSY or DRQ is set to one, the content of all register bits and fields except BSY and DRQ in the Status and Alternate Status registers is indeterminate. If the host writes to any Command Block register when BSY or DRQ is set to one, the results are indeterminate and may result in the command in progress ending with a command abort error.

When performing PIO transfers, BSY and DRQ shall both be cleared to zero within 400 ns of the transfer of the final byte of data. This assertion signals the completion of a PIO data transfer command.

Table 5: I/O port functions and selection address

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	×	×	×	Data bus high impedance	Note used
					Control block registers	
N	A	0	×	×	Data bus high impedance	Note used
N	A	1	0	×	Data bus high impedance	Note used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	(see note1)	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number LBA (7:0) (see note 2)	Sector Number LBA (7:0) (see note 2)
A	N	1	0	0	Cylinder Low LBA (15:8) (see note 2)	Cylinder Low LBA (15:8) (see note 2)
A	N	1	0	1	Cylinder High LBA (23:16) (see note 2)	Cylinder High LBA (23:16) (see note 2)
A	N	1	1	0	Device/Head LBA (27:24) (see note 2)	Device/Head LBA (27:24) (see note 2)
A	N	1	1	1	Status	Command
A	A	×	×	×	Invalid address	Invalid address

Key:
A = signal asserted, N = signal negated, × = don't care
NOTES_
1 This register is obsolete. It is recommended that a device not respond to a read of this address. If a device does respond, it shall not drive the DD7 signal to prevent possible conflict with floppy disk implementations.
2 Mapping of registers in LBA translation.

Each register description in the following clauses contain the following format:
ADDRESS – the CS and DA address of the register.
DIRECTION – indicates if the register is read/write, read only, or write only from the host.
ACCESS RESTRICTIONS – indicates when the register may be accessed.
EFFECT – indicates the effect of accessing the register.
FUNCTIONAL DESCRIPTION – describes the function of the register.
FIELD/BIT DESCRIPTION – describes the content of the register.

[Duplicate Data, Error and Feature register]
    During word access, the address space occupied by the Data Register interferes with the space occupied by the Error register and Feature register, and reference cannot be made to these registers. Therefore, the PC Card ATA Standard provides an area where the copy of each register does not duplicate in the contiguous I/O mode and memory map mode. The even-numbered address of the data register is provided in the offset "08h", and the odd-numbered address of the data register is located in the offset "09h". The copy of
Error/Feature register is provided at the ODh.

Duplicate Data register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Word															
Odd Data Byte Only								Even or Even-Odd Data Byte							

Duplicate registers Access

Data register	CE2#	CE#	A0	Offset	Data Bus
Word Data register	0	0	0	0h,8h	D15-D0
Word Data register	0	0	1	1h,9h	D15-D0
Even Byte Data register	1	0	0	0h,8h	D7-D0
Odd Byte Data register	1	0	1	9h	D7-D0
Odd Byte Data register	0	1	×	8h,9h	D15-D8
Error/Feature register	1	0	1	1h,0Dh	D7-D0
Error/Feature register	0	1	×	0h,1h	D15-D8
Error/Feature register	0	0	×	0Ch,0Dh	D15-D8

Initial value of task file register
    After resetting and execution of the Execute Device Diagnostic command, the task file register is initialized as follows:

Sector Count register	01h
Sector Number register	01h
Cylinder Lo register	00h
Cylinder High register	00h
Device/Head register	A0h

3.7 PIO Data Transfers
    Figure 1 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO Transfer Mode 3 or 4 shall power up in a PIO Transfer Mode 0, 1, or 2.
    For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the IDENTIFY DEVICE parameter list.
    IORDY shall be supported when PIO Mode 3 or 4 are the current mode of operation.

Figure 7 : PIO data transfer to/from device

NOTES

1 Device address consists of signals CS0-, CS1- and DA(2:0)

2 Data consists of DD(15:0). For READ LONG and WRITE LONG commands, the transfer of the vendor specific bytes shall be 16 bit transfers with the vendor specific byte in bits 7 through 0. Bits 15 through 8 shall be ignored.

3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

  3-1 Device never negates IORDY: no wait is generated.

  3-2 Device negates IORDY before tA, but causes IORDY to be asserted before tA: no wait generated.

  3-3 Device negates IORDY before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(15:0) for tRD before asserting IORDY.

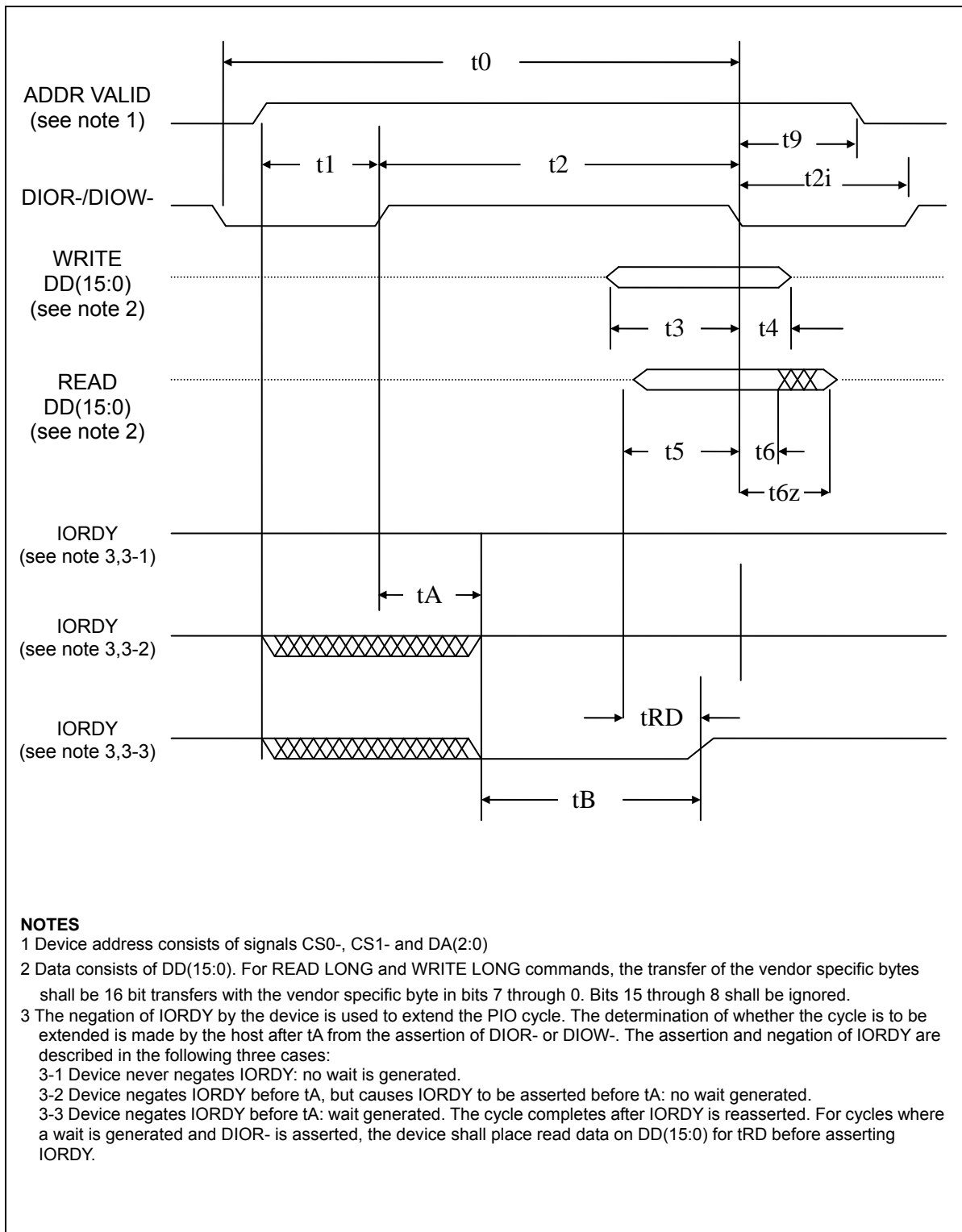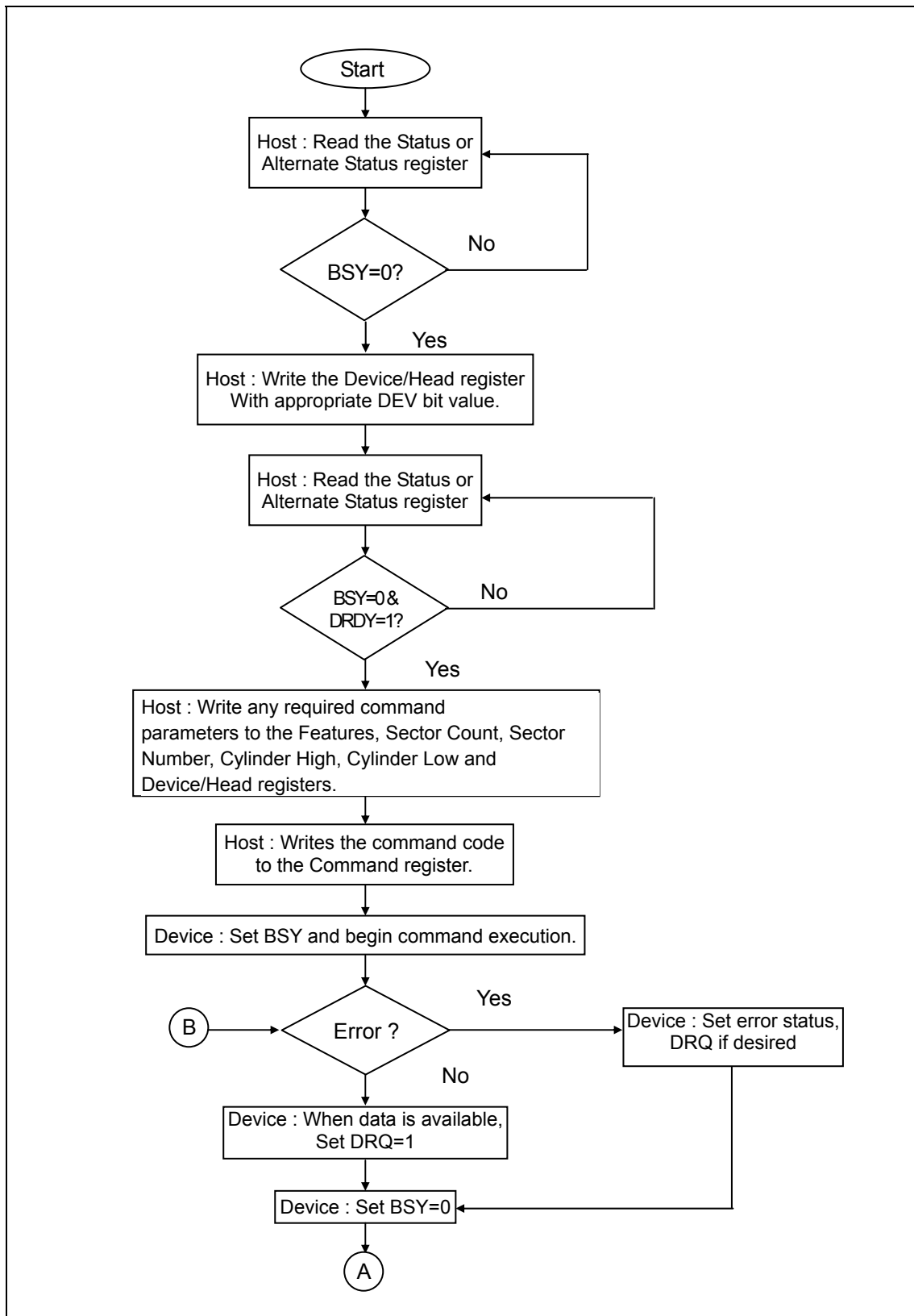**Figure 8 : PIO data transfer in diagram (1)**

Figure 9 : PIO data transfer in diagram (2)

```
                           ( Start )
                               |
                               v
              +--------------------------------+
              | Host : Read the Status or      |<---+
              | Alternate Status register      |    |
              +--------------------------------+    |
                               |                    |
                               v          NO        |
                          / BSY=0 \----------------+
                          \       /
                               | Yes
                               v
              +--------------------------------+
              | Host : Write the Device/Head   |
              | register With appropriate DEV  |
              | bit value.                     |
              +--------------------------------+
                               |
                               v
              +--------------------------------+
              | Host : Read the Status or      |<---+
              | Alternate Status register      |    |
              +--------------------------------+    |
                               |                    |
                               v          NO        |
                       / BSY=0 &  \----------------+
                       \ DRDY=1?  /
                               | Yes
                               v
       +-------------------------------------------+
       | Host : Write any required command         |
       | parameters to the Features, Sector Count, |
       | Sector Number, Cylinder High, Cylinder Low|
       | and Device/Head registers.                |
       +-------------------------------------------+
                               |
                               v
              +--------------------------------+
              | Host : Writes the command code |
              | to the Command register.       |
              +--------------------------------+
                               |
                               v
       +-------------------------------------------+
       | Device : Set BSY and begin command        |
       | execution.                                |
       +-------------------------------------------+
                               |
                               v           Yes
        (B)---->         / Error ? \------------>+--------------------------+
                         \         /             | Device : Set error status|
                               | NO              | DRQ if desired           |
                               v                 +--------------------------+
              +--------------------------------+               |
              | Device: When data is available,|               |
              | Set DRQ=1                      |               |
              +--------------------------------+               |
                               |                               |
                               v                               |
              +--------------------------------+               |
              | Device : Set BSY=0             |<--------------+
              +--------------------------------+
                               |
                               v
                             (A)
```
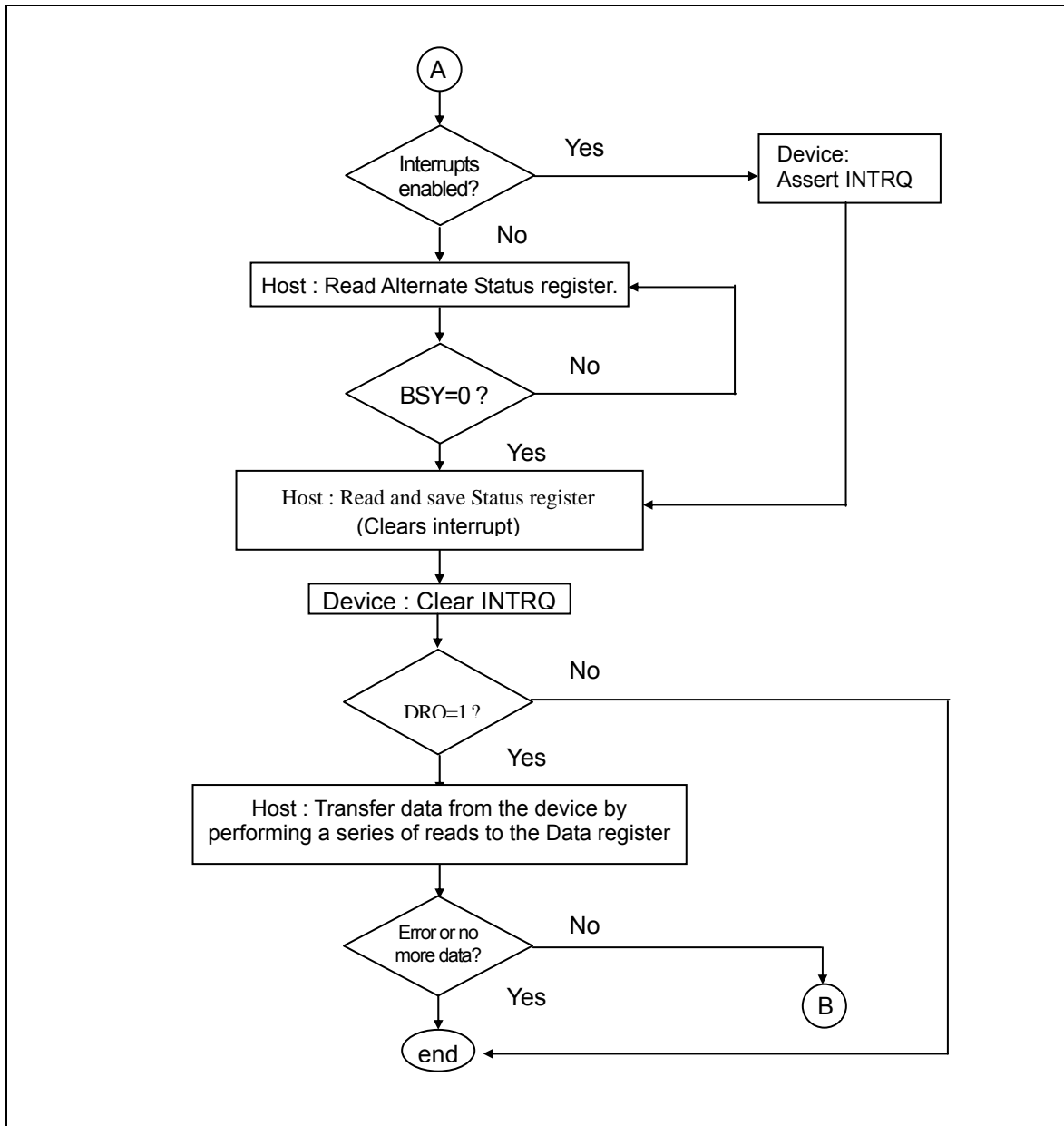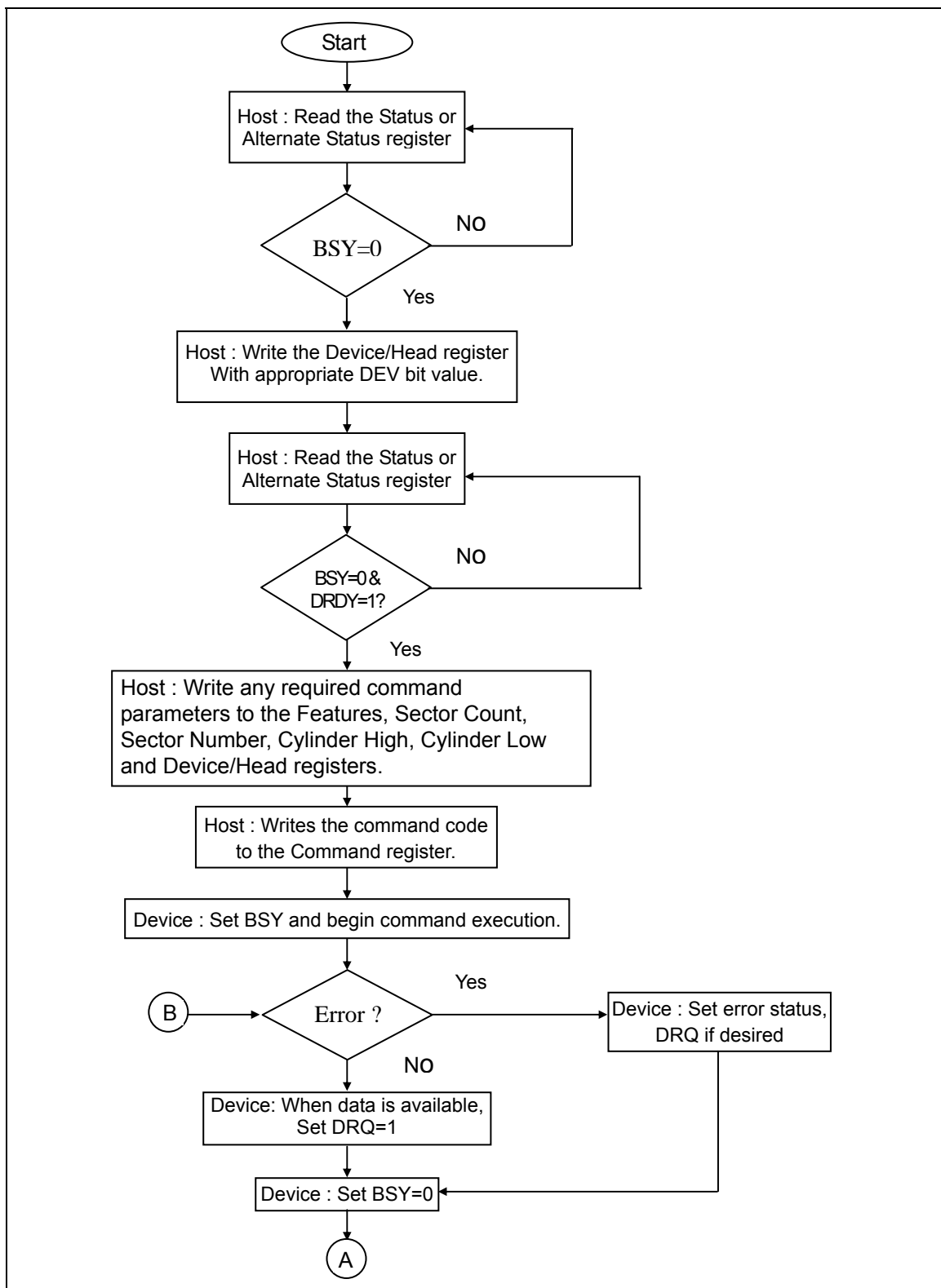
Figure10 : PIO data transfer out diagram (1)
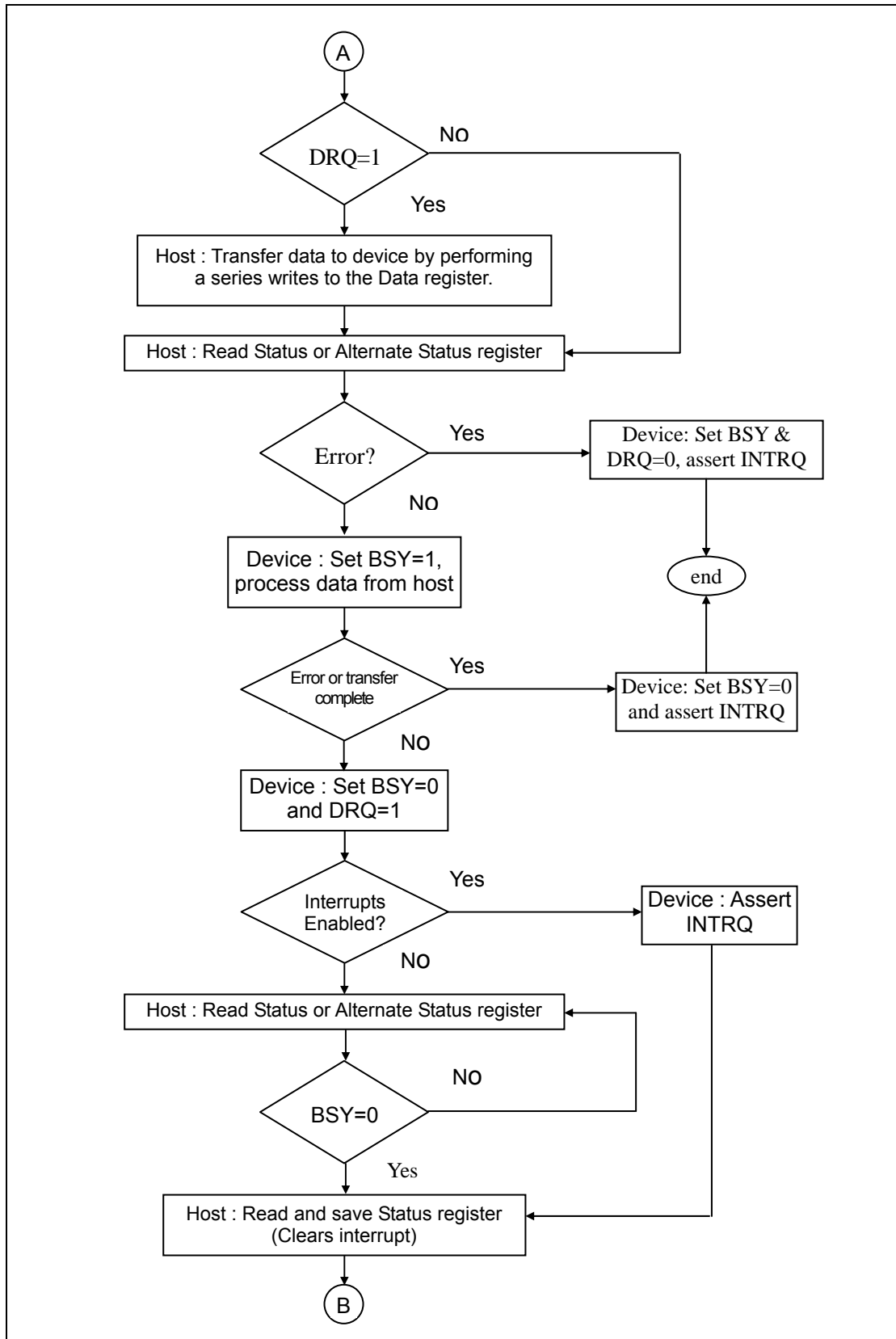
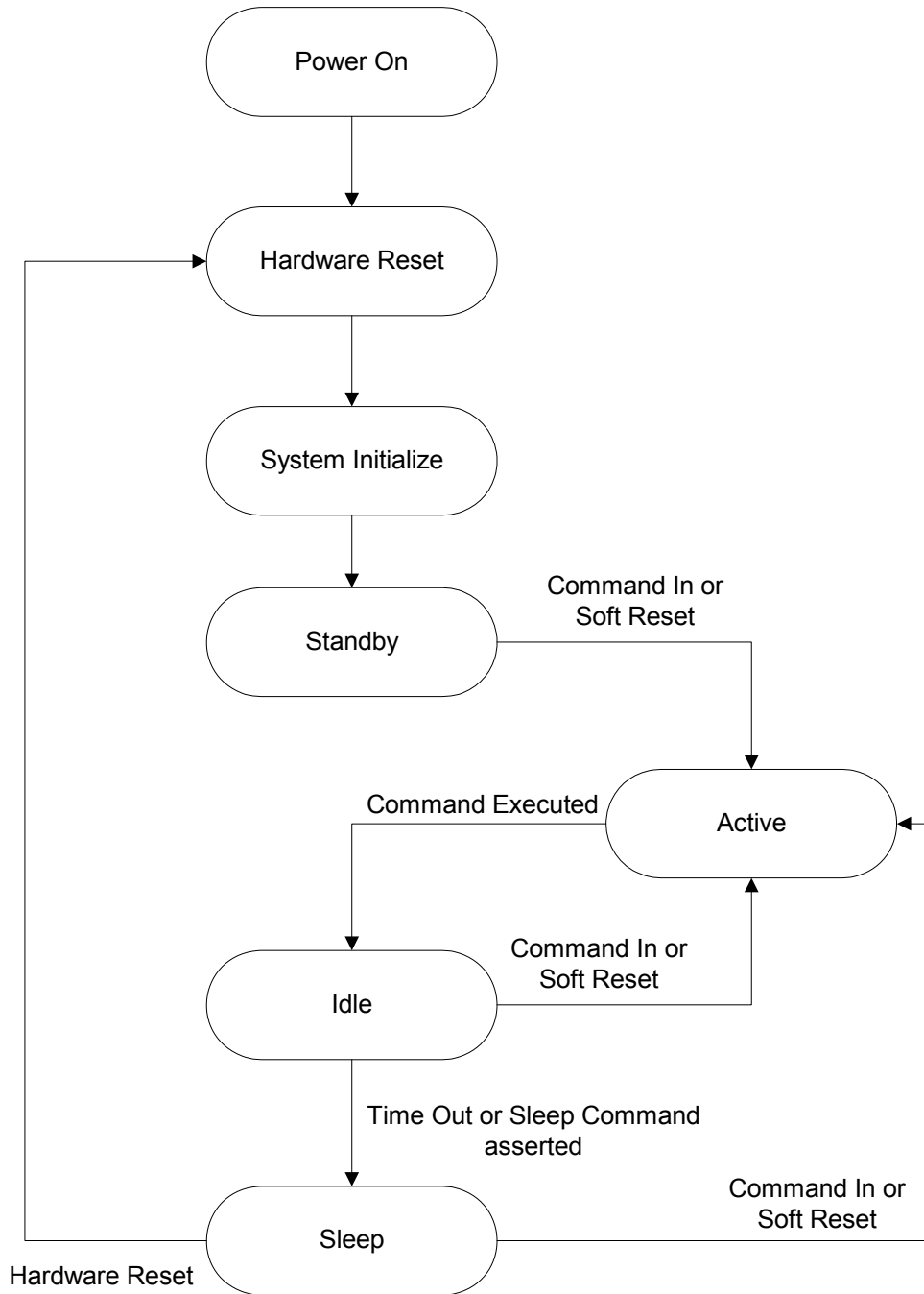**Figure 11 : PIO data transfer out diagram (2)**

Power Saving Flow:


```
                    ┌─────────────┐
                    │  Power On   │
                    └─────────────┘
                           │
                           ▼
                    ┌─────────────┐
                    │Hardware Reset│
                    └─────────────┘
                           │
                           ▼
                    ┌─────────────┐
                    │System Initialize│
                    └─────────────┘
                           │
                           ▼
                    ┌─────────────┐        Command In or
                    │  Standby    │──────── Soft Reset
                    └─────────────┘                    │
                                                       ▼
                  Command Executed              ┌─────────────┐
                    ┌───────────────────────────│  Active     │
                    ▼                            └─────────────┘
              ┌─────────────┐   Command In or
              │   Idle      │─── Soft Reset
              └─────────────┘
                    │
                    │  Time Out or Sleep Command asserted
                    ▼                            Command In or
              ┌─────────────┐                    Soft Reset
              │   Sleep     │────────────────────
              └─────────────┘
         Hardware Reset
```

Figure 12 : Power Saving Flow

3.8 Absolute Maximum Ratings

Table 6: Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
3	Ta	Operating Temperature	-0	+70	℃
4	Tst	Storage Temperature	-40	+85	℃

3.9 DC Specifications

3.9.1 DC Characteristics-1 (Ta=0 to +70℃, V_{CC}= 3.3V ± 10%)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Voltage	VIH	--	2.0	--	V_{CC} +0.3	V
	VIL	--	-0.3	--	0.8	V
Output Voltage IOL = 4mA (*1)	VOH	IOL = -1mA	2.4	--	--	V
	VOL	IOL = 4mA	--	--	0.45	V
Input leakage current (*2)	ILK	VIH = VDD / VIL = GND	-10	--	10	uA
Sleep current (*3)	ISP	Control signal = V_{CC} – 0.2	--	3	--	mA
Sector read current (*4,*3)	ISR(DC)	Control signal = V_{CC} – 0.2	--	10	--	mA
	ISR(Peak)		--	20	--	mA
Sector write current (*5,*3)	ISW(DC)	Control signal = V_{CC} – 0.2	--	15	--	mA
	ISW(Peak)		--	30	--	mA

3.9.2 DC Characteristics-1 (Ta=0 to +70℃, V_{CC}= 5.0V ± 10%)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Voltage	VIH	--	2.0	--	V_{CC} +0.3	V
	VIL	--	-0.3	--	0.8	V
Output Voltage IOL = 4mA (*1)	VOH	IOL = -1mA	2.4	--	--	V
	VOL	IOL = 4mA	--	--	0.45	V
Input leakage current (*2)	ILK	VIH = VDD / VIL = GND	-10	--	10	uA
Sleep current (*3)	ISP	Control signal = V_{CC} – 0.2	--	3	--	mA
Sector read current (*4,*3)	ISR(DC)	Control signal = V_{CC} – 0.2	--	15	--	mA
	ISR(Peak)		--	30	--	mA
Sector write current (*5,*3)	ISW(DC)	Control signal = V_{CC} – 0.2	--	20	--	mA
	ISW(Peak)		--	40	--	mA

Note :

1. Measured for static state.

2. Except pulled up input/output pin.

3. Power dissipation is reference value on the assembled flash card, including the flash memory.

4. Measured during sector read transfer.

5. Measured during sector write transfer.

3.10 ATA Commands

The following table lists the ATA commands that are supported

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check power mode	E5H, 98H	—	—	—	—	Y	—	—
2	Execute drive diagnostic	90H	—	—	—	—	—	—	—
3	Format track	50H	—	Y	—	Y	Y	Y	Y
4	Identify Device	ECH	—	—	—	—	Y	—	—
5	Idle	E3H, 97H	—	Y	—	—	Y	—	—
6	Idle immediate	E1H, 95H	—	—	—	—	Y	—	—
7	Initialize drive parameters	91H	—	Y	—	—	Y	Y	—
8	Read buffer	E4H	—	—	—	—	Y	—	—
9	Read multiple	C4H	—	Y	Y	Y	Y	Y	Y
10	Read long	22H, 23H	—	—	Y	Y	Y	Y	Y
11	Read sector(s)	20H, 21H	—	Y	Y	Y	Y	Y	Y
12	Read verify sector(s)	40H, 41H	—	Y	Y	Y	Y	Y	Y
13	Recalibrate	1XH	—	—	—	—	Y	—	—
14	Seek	7XH	—	—	Y	Y	Y	Y	Y
15	Set features	EFH	Y	—	—	—	Y	—	—
16	Set multiple mode	C6H	—	Y	—	—	Y	—	—
17	Set sleep mode	E6H, 99H	—	—	—	—	Y	—	—
18	Stand by	E2H, 96H	—	—	—	—	Y	—	—
19	Stand by immediate	E0H, 94H	—	—	—	—	Y	—	—
20	Write buffer	E8H	—	—	—	—	Y	—	—
21	Write long	32H, 33H	—	—	Y	Y	Y	Y	Y
22	Write multiple	C5H	—	Y	Y	Y	Y	Y	Y
23	Write sector(s)	30H, 31H	—	Y	Y	Y	Y	Y	Y
24	Write verify	3CH	—	Y	Y	Y	Y	Y	Y

Notes:

FR : Feature Register

SC : Sector Count register (00H to FFH, 00H means 256 sectors)

SN : Sector Number register

CY : Cylinder Low/High register

DR : Drive bit of Drive/Head register

HD : Head No. (0 to 15) of Drive/Head register

Y : Used for the command

— : Not used for the command

Check power mode

PROTOCOL - Non-data command

The Sector Count register is set to 0 (00h) if the device in Standby mode, and to 255 (FFh) if the device is in Active mode.

Execute drive diagnostic

PROTOCOL - Non-data command.

This command shall performs the internal diagnostic tests of the device. The test result is written to the Error register. The Dev bit in the Device/Head register is ignored for this command.

Format track

PROTOCOL - PIO data out.

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h).

Identify Device

PROTOCOL - PIO data in.

This command sets up the device's parameter information (256 words) as specified in section 4.3 in the sector buffer.

Idle, Idle immediate

PROTOCOL - Non-data command.
This command causes the device to enter the Idle Mode.

Initialize drive parameters

PROTOCOL - Non-data command.
This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1, per logical cylinder for the current CHS translation mode.

Read buffer

PROTOCOL - PIO data in.
This command enables the host to read the current contents of the device's sector buffer.

Read multiple

PROTOCOL - PIO data in.
This command is identical to the Read Sector(s) command since only a multiple setting of 1 is supported.

Read long

PROTOCOL - PIO data in

This command performs similarly to the Read Sector(s) command except that it returns the data and a number of vendor specific bytes appended to the data field of the desired sector.Only single sector Read Long operations are supported.

Read sector(s)

PROTOCOL - PIO data in.
This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

Read verify sector(s)

PROTOCOL - Non-data command.
This command is identical to the Read Sector(s) command, except that the DRQ bit is never set, and no data is transferred to the host.

Recalibrate

PROTOCOL - Non-data command.
This command is effectively a NOP command and is provided for compatibility purposes.

Seek

PROTOCOL - Non-data command.
This command is effectively a NOP command although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

Set features

PROTOCOL - Non-data command.

This command is used by the host to establish parameters which affect the execution of certain device features. The following features are supported:

01h	Enable 8-bit data transfers.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8-bit data transfer.
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility.
9Ah	Set the host current source capability.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Set multiple mode

PROTOCOL - Non-data command.

This command establishes the block count for Read Multiple and Write Multiple commands. Only a multiple setting of 1 is supported.

Set sleep mode

PROTOCOL - Non-data command.

This command causes the device to enter Sleep Mode.

Stand by, Stand by immediate

PROTOCOL - Non-data command.

This command causes the device to enter the Standby Mode.

Write buffer

PROTOCOL - PIO data out.

This command enables the host to overwrite the contents of the device's sector buffer.

Write long

PROTOCOL - PIO data out.

This command is similar to the Write Sector(s) command except that it writes the data and the vendor specific bytes as supplied by the host; the device does not generate the vendor specific bytes itself.Only single sector Write Long operations are supported.

Write multiple

PROTOCOL - PIO data out.

This command is identical to the Write Sector(s) command since only a multiple setting of 1 is supported.

Write sector(s)

PROTOCOL - PIO data out.

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors.

Write verify

PROTOCOL - PIO data out.

This command is similar to the Write Sector(s) command except that each sector is verified before the command is completed.

4. Introduction of DiskOnModule

4.1 What is DiskOnModule?

PQI's DiskOnModule is a storage device based on flash memory technology, which emulates an ordinary magnetic hard disk. The DiskOnModule series products provide an all in one module solution for solid-state flash disk. The DiskOnModule is suitable for use in portable and embedded systems which have limited space and power consumption.

Unlike standard IDE drives, no signal cable and extra, special space is required. The DiskOnModule is a solid-state solution for IDE Hard Disk drive, which has no moving parts. That provides a good stability in a moving system.The DiskOnModule products are also free from extra and special algorithm or some firmware driver. Just plug the DiskOnModule into the IDE slot and play it,users can play the DiskOnModule as same as the Hard Disk Drives.

The DiskOnModule family provides the capacities ranging from 32MB up to 8GB. In the future, the capacity will be increased up to 16GB.

4.2 About Our Flash Management

In order to gain the best management for flash memory, PQI **DiskOnModule** supports an efficient and swift algorithm. Due to the life of flash memory is limited, PQI try to increase the life of our flash product through the following arrangement. There are some blocks are reserved in flash memory and these blocks would not be used in normal operation. Once any block is unstable, one of these reserved blocks will replace it and the data of the fail block would be transferred to the reserved block for keeping the data's accuracy. After we used the above arrangement in flash memory, the life of the device will be longer than the device without it. When all of the reserved blocks have replaced the bad blocks, the device will be locked automatically to prevent programming, but the data can still be read out for back up.

Because the block of flash memory has a limited life, when the host writes data in the same address, PQI **DiskOnModule** does not to program data into the same physical place of the flash memory in purpose, our algorithm will get the data precisely when the host wants to read the data.

ECC (Error Correction Code) feature also be built in our hardware and firmware. ECC ensured the accuracy of the data, and decreased the effect of the cross talking on the bus.

5. Installation Guide

Before You Begin

To protect your DOM from static discharge by making sure you are well grounded before touching the DOM. We recommend wearing a grounded wrist strap throughout the installation process.

STEP 1

1. Make sure your computer is turned off before you open the case.
2. Plug the DOM carefully into the IDE slot on your computer or host adapter.
  Caution: Make sure to align pin1 on the computer or host adapter interface connector with pin 1 on your DOM. Pin 1 is indicated by a triangle on the DOM connector.
3. Connect the power cable of the DOM to an unused power connector of the computer.
  Caution: If you need to remove your DOM, use **BOTH HANDS** to carefully pull out it.
4. Check all cable connections and then replace your computer cover.

STEP 2

Before you format or partition your new DOM, you must configure your computer's BIOS so that the computer can recognize your new DOM.

1. Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as DELETE,ESC, or F1, during startup. See your computer manual for details. Press the appropriate key to run the system setup program.
2. If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option. (If you use Normal/CHS mode to partition your DOM, you can get the maximum formatted capacity.)
   This allows your computer to configure itself automatically for your new DOM.
   If your BIOS does not provide automatic drive detection, select "User-defined" drive setting and enter the CHS values from the table.
   BIOS Settings (see specification)
   Capacity   Cylinders   Heads   Sectors
   (unformatted)
3. Save the settings and exit the System Setup program.
   (your computer will automatically reboot)
   After you configure your computer, you can use the standard DOS commands to partition and format your DOM, as described below.

STEP 3

To partition your new DOM, for example use Microsoft$^®$ DOS program :
1. Insert a bootable DOS diskette into your diskette drive and restart your computer.
2. Insert a DOS program diskette that contains the **FDISK.EXE** and **FORMAT.COM** programs into your diskette drive. Use the same DOS version that is on your bootable diskette. At the A: prompt, type **FDISK** and press **ENTER***.*
3. If you have two **IDE** devices installed, the **FDISK** menu displays five options. Option five allows you to select the drive you want to partition. Make sure that your new drive is selected.
4. Select "Create DOS partition or logical DOS drive" by pressing **1**. Then press **ENTER**.
5. Select "**Create primary DOS partition**" by pressing 1 again. Then press ENTER. Create your first drive partition. If you are creating a partition that will be used to boot your computer (drive C), make sure that the partition is marked active.
6. Create an extended partition and additional logical drives as necessary, until all the space on your new hard drive has been partitioned.
7. When the partitioning is complete, **FDISK** reboots your computer.
   Caution: Make sure to use the correct drive letters so that you do not format a drive that already contains data.
8. At the A: prompt, type **format c:/s**, where c is the letter of your first new partition, Repeat the format process for all the new partitions you have created.
9. After you format your DOM, it is ready to use.

6.Format

For DOS Operating System：

- Before you format or partition your new DiskOnModule, you must configure your computer's BIOS so that the computer can recognize your new DiskOnModule.

1. Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as DELETE, ESC, or F1, during startup. See your computer manual for details. Press the appropriate key to run the system setup program.

2. If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option. (If you use Normal/CHS mode to partition your DOM, you can get the maximum formatted capacity.)

   This allows your computer to configure itself automatically for your new DiskOnModule.

   If your BIOS does not provide automatic drive detection, select "User-defined" drive setting and enter the CHS values from the table.

BIOS Settings (see specification)
Capacity　　　Cylinders　　　Heads　　　Sectors　(unformatted)

3. Save the settings and exit the System Setup program.
(Your computer will be automatically rebooted.)

For Windows Operating System：

- To partition your new DOM, for example use Microsoft WindowsXP and WindowsXP
embedded system：

1. Click the 『Start』→『Control Panel』→『Administrative Tools』→『Computer Management』
then select 『Storage』→『Disk Manager』 to setup the file format.

2. Select "FAT or NTFS" format for user.
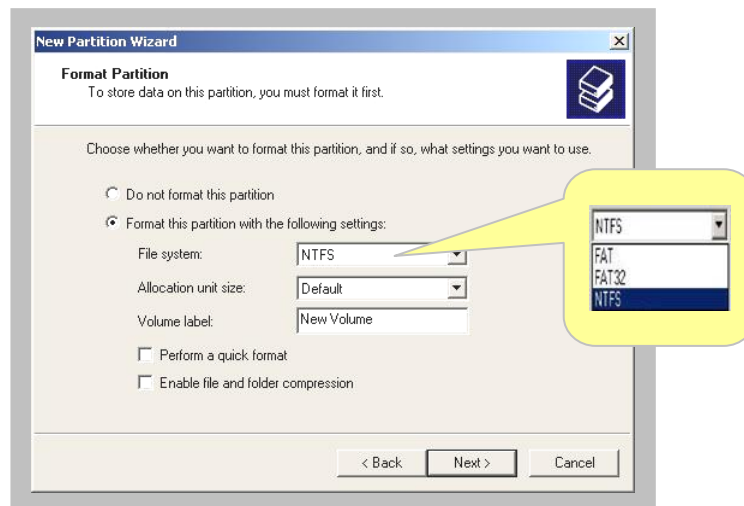
7. Troubleshooting

7.1 BIOS can not identify DiskOnModule
7.1.1 Check Power Cable Status
7.1.2 Check Connector status
7.1.3 Check the Power Voltage (5V or 3.3V)

7.2 DOM can not boot the system
7.2.1 Check BIOS setting
7.2.2 Reinstall your system

Notice *Please contact your closest PQI's office for verifying your other troubles.*

8. Ordering Information

Table 7: DiskOnModule Ordering Information

P/N	Capacity (Max)
DJ0**032M**$*_1$22R$*_2$ **D**$*_3$0	6GB

*1：032M:32MB, 064M:64MB, 128M:128MB, 256M:256MB, 512M:512MB, 010G:1GB, 020G:2GB, 040G:4GB, 060G:6GB

  * 6GB without write protect switch solution.

[*]2：R: Industrial type

[*]3:：Flash Density
  D:32MB, E:64MB, F:128MB, I:256MB, L:512MB, N:1GB, P:2GB

[*]4：DJ0*032M*22R*D*0(WP): With Write Protect Switch
  DJ0*032M*22R*D*0   : Without Write Protect Switch

9. Contact Information

●   CoreSolid Storage Corporation, a TDK-PQI storage business company, is represented for PQI DOM, Industry CF, and SSD products on design and business operation from Oct. 1, 2007 effectively.

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